REMARKS

This responds to the Office Action mailed on April 23, 2008.

No claims are amended, canceled, or added; as a result, claims 1-25 remain pending in this application.

§102 Rejection of the Claims

Claims 1-25 were rejected under 35 USC § 102(b) as being anticipated by Grimes (U.S. 5,684,979; hereinafter "Grimes"). Applicant respectfully traverses the 35 U.S.C. § 102(b) rejection because Grimes fails to teach or suggest all the elements of the claims.

Applicant reiterates, and incorporates by this reference, the previous arguments of the last two Office Action responses as they are equally applicable here. In particular, Applicant respectfully submits that the claimed invention provides solutions where memory initialization and testing is performed in parallel at the memory module level rather than at the CPU or memory controller level.

Applicant refers the Examiner's attention to FIG. 1 which illustrates how the processor 102 is distinct from the memory controller 104. Further, the memory modules 112, 114, 116 are distinct from the memory controller 104. Applicant's specification provides description as to the details of a processor in the paragraph beginning on line 17 of page 4. Description of the memory controller is found in the paragraph beginning at line 28 of page 4 and the following paragraphs. Description of the memory modules is found in the paragraph beginning at line 22 of page 5 and the following paragraphs. These descriptive portions of the specification, among others, provide background and definitions for the elements of the claims and highlight how the memory initialization and testing is performed by memory modules in response to commands originating with a processor and may be communicated via a memory controller. Further, FIG. 2, and its description beginning at line 7 of page 8, illustrates how a memory module includes memory storage units.

Applicant respectfully submits that this highlights what a memory module, as included in the claims, is and is not. A memory module is not a memory controller 36 or a CPU 30 as is described in Grimes. Further, a memory module may include memory storage units, but is more than a portion of system memory. Thus, Applicant submits that the concept of a memory module

is not disclosed, taught, or suggested in any manner within Grimes. A memory module, as claimed, provides an additional level of memory management and allows for finer grained parallel memory initialization and testing.

More specifically with regards to Grimes, the Office Action on pages 3 and 4 generally refers to the method illustrated in FIG. 8. FIG. 8 of Grimes is described beginning at col. 5, line 43. Of particular distinction between the present claims and Grimes is within the first paragraph of the FIG. 8 description at col. 5, lines 45-49, which recites:

"The flow chart of FIG. 8 broadly described the initialization process which is performed by the CPU 30 in accordance with memory initialization firmware stored in the ROM 42 and transferred to the L1 cache in CPU 30 for execution."

This clearly provides that the memory initialization is performed by the CPU 30 which, when considered in view of the present invention would indicate serialized memory initialization and not parallel memory initialization and testing as claimed. Further, the present claims provide memory modules that perform the memory initialization and testing.

Thus, for at least these reasons, Applicant respectfully submits that Grimes fails to teach or suggest all the limitations of the claims 1-25, and in particular the memory modules included in each of the independent claims 1, 5, 8, 12, 16, and 21.

Applicant respectfully requests withdrawal of the 35 U.S.C. § 102(b) rejections and allowance of claims 1-25.

RESPONSE UNDER 37 CFR § 1.111

Serial Number: 10/676,137 Filing Date: September 30, 2003

Title: DISTRIBUTED MEMORY INITIALIZATION AND TEST METHODS AND APPARATUS

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney ((612) 349-9592) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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Page 10 Dkt: 884.A46US1

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